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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,699	07/29/2004	Somasekar JAYARAMAN	TI-37107	4698

23494 7590 10/20/2006

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EXAMINER

PARIHAR, SUCHIN

ART UNIT PAPER NUMBER

2825

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,699	JAYARAMAN ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed 8/10/2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is response to application 10/710,699, filed on 7/29/2004, amendment filed on 8/10/2006. Claims 1, 5 and 11 are currently amended. Claims 1-12 are pending in this application.

Applicant's remarks filed 8/10/2006 have been fully considered but they are not persuasive. The applicable rejections from the prior office action are incorporated herein.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. **Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 102(b)** as being anticipated by Salem et al. (5,636,130).

3. With respect to claims 1 and 7, Salem teaches a method and a machine readable medium carrying one or more sequences of instructions to determine whether an integrated circuit operates at a clock speed (Col 1, lines 12-28, i.e. determining design's clock speed), said integrated circuit comprising a combinatorial element, wherein execution of said one or more sequences of instructions (Col 6, lines 42-49, i.e. sequences of instructions) by one more processors contained in said system causes said one or more processors to perform the actions of, and said method comprising: determining a load offered by said combinatorial element when an output path of said

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combinatorial element switches in response to a vector provided as an input to said combinatorial element (Col 4, lines 1-10 and Col 1, lines 60-66, i.e. determining the load associated with the selected gate, wherein gate switches states in response to a signal change on its input, Note: a state-switch on a combinatorial element [i.e. gate] may or may not cause a change on the output path); and performing a timing analysis of said integrated circuit by associating said load to a prior element driving said combinatorial element (Col 3, lines 20-38, and Col 2, lines 25-43, i.e. discussion of timing analyzer),(also see Col 7, lines 37-40, i.e. the load associated).

4. With respect to claims 2 and 8, Salem teaches all the elements of claims 1 and 7, from which the claims depend. Salem teaches: determining another load offered by said combinatorial element when an output path of said combinatorial element does not switch in response to a vector provided as an input to said combinatorial element (Col 4, lines 1-10 and Col 1, lines 60-66, i.e. determining the load associated with the selected gate, wherein gate switches states in response to a signal change on its input, Note: a state-switch on a combinatorial element [i.e. gate] may or may not cause a change on the output path); and performing another timing analysis of said integrated circuit by associating said another load to said prior element (Col 3, lines 20-38, and Col 2, lines 25-43, i.e. discussion of timing analyzer, wherein load and input rise time are in association, and input rise time is associated with a gate immediately preceding the gate under consideration).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 3, 4, 9 and 10 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Salem et al. (5,636,130) in view of Sun et al. (US PG Pub 2005/0268263).

7. With respect to claims 3 and 9, Salem teaches all the elements of claims 2 and 8, from which the claims depend respectively. Salem does not teach: said timing analysis is performed when said integrated circuit is being analyzed for hold time violations of sequential elements contained in said integrated circuit. However, Sun teaches: said timing analysis is performed when said integrated circuit is being analyzed for hold time violations of sequential elements contained in said integrated circuit (pg 1, paragraph [0010] and pg 2, paragraph [0030], i.e. in order to fix hold time violations of sequential circuit cells, timing analysis is performed on the circuit design). It would have been obvious to one of ordinary skill in the art to incorporate Sun into the invention of Salem because Sun improves the invention of Salem by giving consideration to hold time and setup time violations that may be created by gate propagation delays that are either too short or too long (see pg 1, paragraph [0006]).

8. With respect to claims 4 and 10, Salem teaches all the elements of claims 2 and 8, from which the claims depend respectively. Salem does not teach: said timing analysis is performed when said integrated circuit is being analyzed for setup time violations of sequential elements contained in said integrated circuit. However, Sun teaches: said timing analysis is performed when said integrated circuit is being analyzed for setup time violations of sequential elements contained in said integrated circuit (pg 1, paragraph [0006], i.e. violation of setup time requirements for sequential cells). It would have been obvious to one of ordinary skill in the art to incorporate Sun into the invention of Salem because Sun improves the invention of Salem by giving consideration to hold time and setup time violations that may be created by gate propagation delays that are either too short or too long (see pg 1, paragraph [0006]).

9. **Claims 5, 6, 11 and 12 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Salem et al. (5,636,130) in view of Sun et al. (US PG Pub 2005/0268263) and in further view of Van Brunt (4,527,249).

10. With respect to claims 5 and 11, Salem teaches a method for characterizing a load offered by a cell on an input pin, wherein said cell is contained in a library, said method, and machine readable medium comprising: measuring a capacitance of said pin when said pin when said first set of input vectors are applied to said combinatorial element (Col 4, lines 1-6, i.e. determine the load [capacitance] associated with the selected gate –in light of Col 1, lines 60-67, i.e. response to signal change on input pin); and associating said capacitance to said pin if said cell is to be characterized for setup time violation (Col 7, lines 35-40, i.e. discussion of gate capacitance getting so large as

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to increase gate's propagation time, which is directly related to setup and hold time violations). Salem does not teach the relationship between a changing propagation time and setup/hold time violations. However, Sun teaches the relationship between a changing propagation time and setup/hold time violations (pg 1, paragraph [0006], i.e. discussion of setup and hold time requirements). Salem in view of Sun does not teach: determining a first set of input vectors that would cause an output path of a combinatorial element to switch, wherein said combinatorial element is contained in said first cell and connected to said input pin. However, Van Brunt teaches: determining a first set of input vectors that would cause an output path of a combinatorial element to switch, wherein said combinatorial element is contained in said first cell and connected to said input pin (Col 9, lines 43-69, i.e. discussion of using a particular gate's input values and assigned truth table to determine whether an output changes). It would have been obvious to one of ordinary skill in the art to incorporate Sun and Van Brunt into the invention of Salem because: Sun improves the invention of Salem by giving consideration to hold time and setup time violations that may be created by gate propagation delays that are either too short or too long (see pg 1, paragraph [0006]); and Van Brunt improves the invention of Salem by providing a method for which to determine which input values cause a gate to switch states in response to a signal change on time input pin(s) (see Salem, Col 1, lines 60-68, i.e. discussion of switching states, and its relationship to propagation delay).

11. With respect to claims 6 and 12, Salem in view of Sun and in further view of Van Brunt teach all the limitations of the claims from which they depend, respectively.

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Salem teaches: measuring a capacitance of said pin when said second set of input vectors are applied to said combinatorial element (); and associating said capacitance to said pin if said cell is to be characterized for hold time violation (Col 7, lines 35-40, i.e. discussion of gate capacitance getting so large as to increase gate's propagation time, which is directly related to setup and hold time violations). Salem does not teach the relationship between a changing propagation time and setup/hold time violations. However, Sun teaches the relationship between a changing propagation time and setup/hold time violations (pg 1, paragraph [0006], i.e. discussion of setup and hold time requirements). Salem in view of Sun does not teach: determining a second set of input vectors that would not cause said output path to switch. However, Van Brunt teaches: determining a second set of input vectors that would not cause said output path to switch (Col 9, lines 43-69, i.e. discussion of using a particular gate's input values and assigned truth table to determine whether an output changes).

Response to Arguments

12. Applicant's remarks filed 7/28/2006 have been fully considered but they are not persuasive.

13. Applicant asserts that the prior art made of record does not teach or suggest: determining a load offered by said combinatorial element when an output path of said combinatorial element switches in response to a vector provided as an input to said combinatorial element. Examiner disagrees with this assertion.

Examiner points out that Salem teaches: determining a load offered by said combinatorial element (i.e. determining a load associated with a selected gate, Col 4,

lines 3-5) when an output path of said combinatorial element switches in response to a vector provided as an input to said combinatorial element (i.e. gate switches in response to a signal change on its input pin, Col 1, lines 64-66).

14. Applicant asserts that nothing in Salem shows or suggests the utilization of a different load for combinatorial element when the output path switches in response to vector. Applicant goes on to say that nothing shows or suggests that these results [i.e. load and rise time] vary upon whether or not the combinatorial element is made to switch or not. Examiner disagrees with this assertion.

Examiner points out that Salem suggests that the load may change if the propagation time of a gate changes because Salem states that propagation delay of a gate is a function of input rise time and load (Col 2, lines 29-31). Also, Salem suggests that when the gate switches, its propagation time may change, thereby changing the load measured on that gate during the gate state change.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


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